

CLAIMS

What is claimed is:

1 1. A memory module for an embedded PC system, the memory module
2 comprising:
3 a NAND interface device adapted to be coupled to a first chip select of a
4 dedicated SDRAM bus; and
5 at least one NAND memory device coupled to the NAND interface device,
6 wherein the first chip select is utilized to access the NAND memory device via the
7 NAND interface device, and wherein the NAND interface device and the at least one
8 NAND memory device function substantially as a hard disk in the embedded PC system.

1 2. The memory module of claim 1 further comprising at least one
2 synchronous dynamic random access memory (SDRAM) device adapted to be coupled to
3 a second chip select of the dedicated SDRAM bus, wherein the second chip select is
4 utilized to access the at least one SDRAM device.

1 3. The memory module of claim 2 wherein the at least one SDRAM device is
2 coupled to a first side of the memory module and wherein the at least one NAND
3 memory device is coupled to a second side of the memory module.

1 4. The memory module of claim 2 wherein the at least one SDRAM device
2 and the NAND interface device can be adapted to be soldered directly to the dedicated

3 SDRAM bus, and wherein the at least one NAND memory device can be adapted to be
4 soldered directly to the NAND interface device.

1 5. The memory module of claim 1 wherein the NAND interface device can
2 be adapted to be soldered directly to the dedicated SDRAM bus, and wherein the at least
3 one NAND memory device can be adapted to be soldered directly to the NAND interface
4 device.

1 6. The memory module of claim 1 wherein the memory module is adapted to
2 be coupled to a dual inline memory module (DIMM) slot.

1 7. The memory module of claim 1 wherein the memory module is a dual
2 inline memory module (DIMM).

1 8. An embedded PC system comprising:
2 a processor;
3 a dedicated SDRAM bus coupled to the processor; and
4 a memory module coupled to the SDRAM bus, the memory module comprising:
5 a NAND interface device adapted to be coupled to a first chip select of the
6 dedicated SDRAM bus; and
7 at least one NAND memory device coupled to the NAND interface device,
8 wherein the first chip select is utilized to access the NAND memory device via the
9 NAND interface device, and wherein the NAND interface device and the at least one
10 NAND memory device function substantially as a hard disk in the embedded PC system.

1 9. The memory module of claim 8 further comprising at least one
2 synchronous dynamic random access memory (SDRAM) device adapted to be coupled to
3 a second chip select of the dedicated SDRAM bus, wherein the second chip select is
4 utilized to access the at least one SDRAM device.

1 10. The memory module of claim 9 wherein the at least one SDRAM device is
2 coupled to a first side of the memory module and wherein the at least one NAND
3 memory device is coupled to a second side of the memory module.

1 11. The memory module of claim 9 wherein the at least one SDRAM device
2 and the NAND interface device can be adapted to be soldered directly to the dedicated
3 SDRAM bus, and wherein the at least one NAND memory device can be adapted to be
4 soldered directly to the NAND interface device.

1 12. The system of claim 8 wherein the NAND interface device can be adapted
2 to be soldered directly to the dedicated SDRAM bus, and wherein the at least one NAND
3 memory device can be adapted to be soldered directly to the NAND interface device.

1 13. The system of claim 8 wherein the memory module is adapted to be
2 coupled to a dual inline memory module (DIMM) slot.

1 14. The system of claim 8 wherein the memory module is a dual inline
2 memory module (DIMM).

1 15. A method for implementing a NAND memory interface, the method
2 comprising:

3 (a) coupling a first chip select to a NAND interface device, wherein the first
4 chip select is from a dedicated SDRAM bus;

5 (b) coupling at least one NAND memory device to the NAND interface
6 device; and

7 (c) utilizing the first chip select to access the at least one NAND memory
8 device via the NAND interface device, wherein the NAND interface device and the at
9 least one NAND memory device function substantially as a hard disk in the embedded
10 PC system.

1 16. The method of claim 15 wherein the first chip select coupling step (a)
2 comprises the step of (a1) soldering the NAND interface device directly to the dedicated
3 SDRAM bus.

1 17. The method of claim 16 wherein the at least one NAND memory device
2 coupling step (b) comprises the step of (b1) soldering the at least one NAND memory
3 device directly to the NAND interface device.

1 18. The method of claim 15 further comprising:

2 (d) coupling a second chip select to at least one SDRAM device, wherein the
3 second chip select is from the dedicated SDRAM bus; and

4 (e) utilizing the second chip select to access the at least one SDRAM device.

1 19. The method of claim 18 further comprising:
2 (f) coupling the at least one SDRAM device to a first side of a memory
3 module; and
4 (g) coupling the at least one NAND memory device to a second side of the
5 memory module.

1 20. The memory module of claim 19 wherein the memory module is a dual
2 inline memory module (DIMM).

1 21. The method of claim 18 wherein the second chip select coupling step (d)
2 comprises the step of (d1) soldering the at least one SDRAM device directly to the
3 dedicated SDRAM bus.

1 22. A computer-readable medium including program instructions for
2 implementing a NAND memory interface, the program instructions comprising:

3 (a) coupling a first chip select to a NAND interface device, wherein the first
4 chip select is from a dedicated SDRAM bus;

5 (b) coupling at least one NAND memory device to the NAND interface
6 device; and

7 (c) utilizing the first chip select to access the at least one NAND memory
8 device via the NAND interface device, wherein the NAND interface device and the at
9 least one NAND memory device function substantially as a hard disk in the embedded
10 PC system.

1 23. The computer-readable medium of claim 22 wherein the first chip select
2 coupling step (a) comprises the step of (a1) soldering the NAND interface device directly
3 to the dedicated SDRAM bus.

1 24. The computer-readable medium of claim 23 wherein at least one NAND
2 memory device coupling step (b) comprises the step of (b1) soldering the at least one
3 NAND memory device directly to the NAND interface device.

1 25. The computer-readable medium of claim 22 further comprising program
2 instructions for:

3 (d) coupling a second chip select to at least one SDRAM device, wherein the
4 second chip select is from the dedicated SDRAM bus; and

5 (e) utilizing the second chip select to access the at least one SDRAM device.

1 26. The computer-readable medium of claim 25 further comprising program
2 instructions for:

3 (f) coupling the at least one SDRAM device to a first side of a memory
4 module; and

5 (g) coupling the at least one NAND memory device to a second side of the
6 memory module.

1 27. The computer-readable medium of claim 26 wherein the memory module
2 is a dual inline memory module (DIMM).

1 28. The computer-readable medium of claim 25 wherein the second chip
2 select coupling step (d) comprises the step of (d1) soldering the at least one SDRAM
3 device directly to the dedicated SDRAM bus.